REMARKS

The foregoing amendment amends claim 24. Pending in the application are claims 1-6 and 24-29, of which claims 1 and 24 are independent. Claims 7-23 have been withdrawn from further consideration. The following comments address all stated grounds for rejection and place the presently pending claims, as identified above, in condition for allowance.

Election/Restrictions

In response to the Examiner's restriction requirement, Applicant elects Group I (claims 1-6 and 24-29). Applicant elects Group I to expedite the prosecution of the pending application and reserves the right to pursue unelected claims in the pending or separate applications.

Objection to Drawings

The drawings are objected to because reference 23 in Fig. 1 should be labeled as "data transmission path" as indicated in the Specification, page 8, lines 3-4. In response to the objection, Applicant has amended Fig. 1 to label reference 23 as "data transmission path." In light of the amendment to the drawings, Applicant submits that the drawings are in condition for allowance.

Claim Rejections Under 35 U.S.C. 112

Claim 24 is rejected under 35 U.S.C. §112 as being indefinite. In response to the rejection, Applicant has amended claim 24 to change "test vector circuit" to "test circuit." In light of the claim amendments, applicant submits that claim 24 is in condition for allowance.

Claim Rejections Under 35 U.S.C. 102

Claims 1 and 24 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,854,801 to Yamada *et al.* ("Yamada"). Applicant respectfully traverses the rejection for the following reasons.

Claim 1 recites *an integrated circuit* that includes a memory array, a test generator and a conversion circuit. The test generator generates a physical address in the memory array and the

conversion circuit converts the physical address in the memory array to a logical address in the memory array.

Claim 24 recites *a semiconductor device* including a test circuit and a conversion circuit coupled to the test circuit. The test circuit provides a physical memory row address for a selected group of memory cells under test to the conversion circuit for conversion of the provided physical memory address to a logical memory address for the selected group of memory cells under test.

Yamada discloses a pattern generation apparatus and method for SDRAM.

Applicant submits that the cited prior art reference fails to disclose each and every element of claims 1 and 24. Applicant submits that Yamada fails to disclose *an integrated circuit* that includes a memory array, a test generator and a conversion circuit, as recited claim 1, and *a semiconductor device* that includes a test circuit and a conversion circuit coupled to the test, as recited in claim 24. The claimed invention relates to built-in self-test (BIST) for use, for example, in a microprocessor that contains a memory array under test. The claimed invention is directed to *an integrated circuit* or *a semiconductor device* in which a test generator and a conversion circuit (claim 1), or a test circuit and a conversion circuit (claim 24), are built for performing built-in self-test testing a memory array. In comparison, Yamada relates to a test pattern generation apparatus for an SDRAM. Yamada discloses that the apparatus includes a pattern generator (10), a wrap conversion (40), scrambles (31, 32) and SDRAM (20). Yamada, however, does not disclose that these elements are built in *an integrated circuit* or *a semiconductor device*, as recited in the claimed invention.

In light of the aforementioned arguments, Applicant respectfully submits that Yamada fails to disclose each and every element of claims 1 and 24. Applicant therefore requests the Examiner withdraw the rejections of claims 1 and 24 under 35 U.S.C. §102(b), and pass the claims to allowance.

Claim Rejections Under 35 U.S.C. 103

Claims 2-6 and 25-29 are rejected under 35 U.S.C. §103(a) as being unpatentable over the Yamada reference. Applicant respectfully traverses the rejection for the following reasons.

Claims 2-6 and 25-29 depend on claims 1 and 24 and add limitations to claims 1 and 24, respectively. Applicant respectfully submits that the cited prior art reference fails to teach or suggest all of the limitations of claims 1 and 24. Applicant submits that Yamada fails to teach suggest a *an integrated circuit* that includes a memory array, a test generator and a conversion circuit, as recited claim 1, and *a semiconductor device* that includes a test circuit and a conversion circuit coupled to the test, as recited in claim 24. Yamada teaches just a test pattern generation apparatus for an SDRAM. Yamada does not teach that the elements of the apparatus including a pattern generator (10), a wrap conversion (40), scrambles (31, 32) and SDRAM (20) are built in *an integrated circuit* or *a semiconductor device*, as recited in the claimed invention.

Applicant therefore submits that Yamada fails to teach or suggest all of the limitations of claims 1 and 24. Claims 2-6 and 25-29, which depend on claims 1 and 24, are not deemed obvious over the Yamada reference. Applicant requests the Examiner withdraw the rejections of claims 2-6 and 25-29 under 35 U.S.C. §103(a), and pass the claims to allowance.

CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue. If, however, the Examiner considers that further obstacles to allowance of these claims persist, we invite a telephone call to Applicant's representative.

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Respectfully submitted,

By _____

Kevin J. Canning
Registration No. 35,470
LAHIVE & COCKFIELD, LLP
28 State Street
Boston, Massachusetts 02109
(617) 227-7400
(617) 742-4214 (Fax)
Attorney for Applicant